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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,416	01/03/2006	Ronald Dekker	NL03 0786 US1	4530

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
08/25/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,416	DEKKER ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2, 5-7 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "semiconductor substrate being substantially confined to an area of the integrated circuit", as recited in claim 1, is unclear as to what is meant by a semiconductor substrate being substantially confined to an area of the integrated circuit since the semiconductor substrate and the integrated circuit are two separate and distinct elements, wherein the integrated circuit is formed inside the semiconductor substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5-7 and 21, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. (6,607,135) in view of Ichige et al. (6,925,008).

Hirai et al. teach in figure 1 and related text an apparatus being a flexible semiconductor device comprising:

a semiconductor substrate (located within chip 2) defining an active area and having a first surface and a second surface, the first surface being opposite the second surface, wherein the semiconductor substrate is formed from a semiconductor layer;

an integrated circuit 2 provided with a plurality of semiconductor elements (inside chip 2) located at the active area of the semiconductor substrate at the first surface of the semiconductor substrate, the semiconductor substrate having a suitable thickness so as to be flexible, wherein the plurality of semiconductor elements are interconnected according to a desired pattern in an interconnect structure,

a support layer 4 of electrically insulating material, and an antenna 3, which is located laterally outside the active area and is electrically connected to the interconnect structure, the antenna and the integrated circuit being supported by the support layer, and

the semiconductor substrate is substantially confined to an area of the integrated circuit and is absent in areas between the antenna and the integrated circuit,

wherein the integrated circuit is devoid of any bond pad structures,

wherein the semiconductor substrate is present only in the active area,

wherein the antenna is an inductor suitable for wireless communication, and

wherein the integrated circuit is substantially surrounded by the inductor.

Hirai et al. do not teach the structure of the integrated circuit, such that the integrated

circuit comprising a mask formed over the second surface of the semiconductor substrate.

Ichige et al. teach in figures 5 and 27 and related text the structure of an integrated circuit, wherein the integrated circuit comprising a mask 18 formed over the second surface of the semiconductor substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the integrated circuit of Hirai et al.'s device such that it is comprising a mask formed over the second surface of the semiconductor substrate, in order to provide better protection to the active area.

The combined device includes a mask substantially confined at the active area over the integrated circuit, because the mask is located only inside the integrated circuit.

Regarding the process limitations of a mask protects the integrated circuit during removal of potions of the semiconductor layer which are not covered by the mask, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new

method is not patentable as a product, whether claimed in product by process claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 21, Hirai et al. teach the antenna and the integrated circuit are on opposite sides of the interconnect structure, because the interconnect structure is located between the antenna and the integrated circuit.

Response to Arguments

Applicant's arguments with respect to claims 1-2, 5-7 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
8/24/2009

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800